

IN THE CLAIMS

1       1. (original) A method for facilitating inter-digital signal processing (DSP) data  
2       communications comprising the steps of:

3              reading a first data structure associated with a block of local memory in a first  
4       DSP processor core in a complex comprising a plurality of DSP processor cores,  
5       wherein said first data structure comprises a first source address indicating a first  
6       address of where data is stored in said local memory of said first DSP processor core,  
7       wherein said first data structure further comprises an indication of a size of a block of  
8       memory, wherein said first data structure further comprises a first destination address  
9       indicating a second address of where data is to be stored in a local memory of a  
10      second DSP processor core; and

11             initiating a transfer of moving data said size of said block of memory located  
12      in said first source address in said local memory of said first DSP processor core to  
13      said first destination address in said local memory of said second DSP processor core.

1       2. (original) The method as recited in claim 1 further comprising the steps of:

2              obtaining a pointer to a second data structure from said first data structure;  
3              reading said second data structure, wherein said second data structure  
4       comprises a second source address of one of a read pointer and a write pointer,  
5       wherein said second data structure further comprises a second destination address of  
6       one of said read pointer and said write pointer.

1       3. (original) The method as recited in claim 2 further comprising the step of:

2             initiating a transfer of said write pointer located in said second source address  
3      in said local memory of said first DSP processor core to said second destination  
4      address in said local memory of said second DSP processor core.

1       4. (original) The method as recited in claim 2 further comprising the step of:  
2              initiating a transfer of said read pointer located in said second source address  
3        in said local memory of said second DSP processor core to said second destination  
4        address in said local memory of said first DSP processor core.

1       5. (original) The method as recited in claim 2 further comprising the steps of:  
2              obtaining a pointer to a third data structure from said second data structure;  
3              reading said third data structure, wherein said third data structure comprises a  
4        third source address of one of a read pointer and a write pointer, wherein said third  
5        data structure further comprises a third destination address of one of said read pointer  
6        and said write pointer.

1       6. (original) The method as recited in claim 5 further comprising the steps of:  
2              initiating a transfer of said write pointer located in said second source address  
3        in said local memory of said first DSP processor core to said second destination  
4        address in said local memory of said second DSP processor core; and  
5              initiating a transfer of said read pointer located in said third source address in  
6        said local memory of said second DSP processor core to said third destination address  
7        in said local memory of said first DSP processor core.

1       7. (original) The method as recited in claim 5 further comprising the steps of:  
2              initiating a transfer of said write pointer located in said third source address in  
3        said local memory of said first DSP processor core to said third destination address in  
4        said local memory of said second DSP processor core; and  
5              initiating a transfer of said read pointer located in said second source address  
6        in said local memory of said second DSP processor core to said second destination  
7        address in said local memory of said first DSP processor core.

1       8. (original) The method as recited in claim 2 further comprising the steps of:  
2           converting a local address of said write pointer to a global address; and  
3           computing said first source address in said first data structure, wherein said  
4       first source address is equal to said size of a block of memory subtracted from said  
5       global address of said write pointer.

1       9. (original) The method as recited in claim 8 further comprising the steps of:  
2           reading said local address of said write pointer; and  
3           copying said local address of said write pointer into an entry in a third data  
4       structure located in said first DSP processor core.

1       10. (original) The method as recited in claim 8 further comprising the steps of:  
2           reading a local address of said read pointer; and  
3           copying said local address of said read pointer into an entry in a third data  
4       structure located in said second DSP processor core.

1       11. (original) A computer program product embodied in a machine readable medium  
2       for facilitating inter-digital signal processing (DSP) data communications comprising  
3       the programming steps of:  
4           reading a first data structure associated with a block of local memory in a first  
5       DSP processor core in a complex comprising a plurality of DSP processor cores,  
6       wherein said first data structure comprises a first source address indicating a first  
7       address of where data is stored in said local memory of said first DSP processor core,  
8       wherein said first data structure further comprises an indication of a size of a block of  
9       memory, wherein said first data structure further comprises a first destination address  
10      indicating a second address of where data is to be stored in a local memory of a  
11      second DSP processor core; and  
12      initiating a transfer of moving data said size of said block of memory located  
13      in said first source address in said local memory of said first DSP processor core to  
14      said first destination address in said local memory of said second DSP processor core.

1       12. (original) The computer program product as recited in claim 11 further  
2 comprising the programming steps of:

3             obtaining a pointer to a second data structure from said first data structure;  
4             reading said second data structure, wherein said second data structure  
5 comprises a second source address of one of a read pointer and a write pointer,  
6 wherein said second data structure further comprises a second destination address of  
7 one of said read pointer and said write pointer.

1       13. (original) The computer program product as recited in claim 12 further  
2 comprising the programming step of:

3             initiating a transfer of said write pointer located in said second source address  
4 in said local memory of said first DSP processor core to said second destination  
5 address in said local memory of said second DSP processor core.

1       14. (original) The computer program product as recited in claim 12 further  
2 comprising the programming step of:

3             initiating a transfer of said read pointer located in said second source address  
4 in said local memory of said second DSP processor core to said second destination  
5 address in said local memory of said first DSP processor core.

1       15. (original) The computer program product as recited in claim 12 further  
2 comprising the programming steps of:

3             obtaining a pointer to a third data structure from said second data structure;  
4             reading said third data structure, wherein said third data structure comprises a  
5 third source address of one of a read pointer and a write pointer, wherein said third  
6 data structure further comprises a third destination address of one of said read pointer  
7 and said write pointer.

1       16. (original) The computer program product as recited in claim 15 further  
2 comprising the programming steps of:

3           initiating a transfer of said write pointer located in said second source address  
4   in said local memory of said first DSP processor core to said second destination  
5   address in said local memory of said second DSP processor core; and

6           initiating a transfer of said read pointer located in said third source address in  
7   said local memory of said second DSP processor core to said third destination address  
8   in said local memory of said first DSP processor core.

1   17. (original) The computer program product as recited in claim 15 further  
2   comprising the programming steps of:

3           initiating a transfer of said write pointer located in said third source address in  
4   said local memory of said first DSP processor core to said third destination address in  
5   said local memory of said second DSP processor core; and

6           initiating a transfer of said read pointer located in said second source address  
7   in said local memory of said second DSP processor core to said second destination  
8   address in said local memory of said first DSP processor core.

1   18. (original) The computer program product as recited in claim 12 further  
2   comprising the programming steps of:

3           converting a local address of said write pointer to a global address; and

4           computing said first source address in said first data structure, wherein said  
5   first source address is equal to said size of a block of memory subtracted from said  
6   global address of said write pointer.

1   19. (original) The computer program product as recited in claim 18 further  
2   comprising the programming steps of:

3           reading said local address of said write pointer; and

4           copying said local address of said write pointer into an entry in a third data  
5   structure located in said first DSP processor core.

1   20. (original) The computer program product as recited in claim 18 further  
2   comprising the steps of:

3           reading a local address of said read pointer; and  
4           copying said local address of said read pointer into an entry in a third data  
5       structure located in said second DSP processor core.

1       21. (original) A system, comprising:  
2           a plurality of digital signal processing (DSP) units;  
3           a direct memory access controller coupled to said plurality of DSP processor  
4       cores, wherein said direct memory access controller comprises:  
5               a memory unit operable for storing a computer program for facilitating  
6       inter-DSP data communications; and  
7               a processor coupled to said memory unit, wherein said processor,  
8       responsive to said computer program, comprises:  
9                 circuitry operable for reading a first data structure associated  
10      with a block of local memory in a first DSP processor core, wherein said first data  
11      structure comprises a first source address indicating a first address of where data is  
12      stored in said local memory of said first DSP processor core, wherein said first data  
13      structure further comprises an indication of a size of a block of memory, wherein said  
14      first data structure further comprises a first destination address indicating a second  
15      address of where data is to be stored in a local memory of a second DSP processor  
16      core; and  
17                 circuitry operable for initiating a transfer of moving data said  
18      size of said block of memory located in said first source address in said local memory  
19      of said first DSP processor core to said first destination address in said local memory  
20      of said second DSP processor core.

1       22. (original) The system as recited in claim 21, wherein said processor further  
2       comprises:  
3           circuitry operable for obtaining a pointer to a second data structure from said  
4       first data structure;  
5           circuitry operable for reading said second data structure, wherein said second  
6       data structure comprises a second source address of one of a read pointer and a write

7 pointer, wherein said second data structure further comprises a second destination  
8 address of one of said read pointer and said write pointer.

1 23. (original) The system as recited in claim 22, wherein said processor further  
2 comprises:

3 circuitry operable for initiating a transfer of said write pointer located in said  
4 second source address in said local memory of said first DSP processor core to said  
5 second destination address in said local memory of said second DSP processor core.

1 24. (original) The system as recited in claim 22, wherein said processor further  
2 comprises:

3 circuitry operable for initiating a transfer of said read pointer located in said  
4 second source address in said local memory of said second DSP processor core to  
5 said second destination address in said local memory of said first DSP processor core.

1 25. (original) The system as recited in claim 22, wherein said processor further  
2 comprises:

3 circuitry operable for obtaining a pointer to a third data structure from said  
4 second data structure;

5 circuitry operable for reading said third data structure, wherein said third data  
6 structure comprises a third source address of one of a read pointer and a write pointer,  
7 wherein said third data structure further comprises a third destination address of one  
8 of said read pointer and said write pointer.

1 26. (original) The system as recited in claim 25, wherein said processor further  
2 comprises:

3 circuitry operable for initiating a transfer of said write pointer located in said  
4 second source address in said local memory of said first DSP processor core to said  
5 second destination address in said local memory of said second DSP processor core;  
6 and

7 circuitry operable for initiating a transfer of said read pointer located in said

8 third source address in said local memory of said second DSP processor core to said  
9 third destination address in said local memory of said first DSP processor core.

1 27. (original) The method as recited in claim 25, wherein said processor further  
2 comprises:

3 circuitry operable for initiating a transfer of said write pointer located in said  
4 third source address in said local memory of said first DSP processor core to said  
5 third destination address in said local memory of said second DSP processor core;  
6 and

7 circuitry operable for initiating a transfer of said read pointer located in said  
8 second source address in said local memory of said second DSP processor core to  
9 said second destination address in said local memory of said first DSP processor core.

1 28. (original) The system as recited in claim 22, wherein said first DSP processor  
2 core comprises:

3 a second memory unit operable for storing a computer program for  
4 performing background tasks; and

5 a second processor coupled to said second memory unit, wherein said second  
6 processor, responsive to said computer program, comprises:

7 circuitry operable for converting a local address of said write pointer  
8 to a global address; and

9 circuitry operable for computing said first source address in said first  
10 data structure, wherein said first source address is equal to said size of a block of  
11 memory subtracted from said global address of said write pointer.

1 29. (original) The system as recited in claim 28, wherein said second processor  
2 further comprises:

3 circuitry operable for reading said local address of said write pointer; and

4 circuitry operable for copying said local address of said write pointer into an  
5 entry in a third data structure located in said first DSP processor core.

1       30. (original) The system as recited in claim 28, wherein said second DSP processor  
2 core comprises:

3           a third memory unit operable for storing a computer program for performing  
4 background tasks; and

5           a third processor coupled to said third memory unit, wherein said third  
6 processor, responsive to said computer program, comprises:

7              circuitry operable for reading a local address of said read pointer; and

8              circuitry operable for copying said local address of said read pointer  
9 into an entry in a third data structure located in said second DSP processor core.